I CLAIM:

1. A method of activating a wordline in a memory device, comprising:

turning on first and second isolation circuits via first and second isolation signals to conductively couple digit lines to a sense amplifier;

turning off the first isolation signal and the first isolation circuit to isolate the digit lines connected to a first memory array from the sense amplifier; and

activating a wordline based on the turning off the first isolation signal.

2. The method of claim 1, wherein activating the wordline includes inputting first isolation signal and a RAS* into a timing circuit.

3. The method of claim 2, wherein activating the wordline includes outputting a signal from the timing circuit to a wordline decoder.

4. The method of claim 3, wherein activating the wordline includes decoupling the wordline from ground and applying a voltage to the wordline.

5. A method of activating a wordline in a memory device, comprising:

turning on first and second isolation circuits via first and second isolation signals to conductively couple pairs of digit lines to a sense amplifier;

turning off the first isolation signal and the first isolation circuit to isolate the pair of digit lines connected to a first memory array from the sense amplifier; and

activating a wordline of a second memory array based on the turning off the first isolation signal.

6. The method according to claim 5, wherein activating the wordline includes holding a constant delta margin between the first isolation signal and wordline activation regardless of the location of the second memory array on an IC chip.

7. The method according to claim 5, wherein activating the wordline includes applying a second signal to a wordline decoder and activating the wordline decoder when both the first isolation signal and the second signal are received in a timing circuit that controls activation of the wordline decoder.

8. The method according to claim 7, wherein applying the second signal includes applying the RAS* signal before applying the first isolation signal to the timing circuit.

9. A method of activating a wordline in a memory device, comprising:
applying RAS* signal to a timing circuit;
applying an ISO signal to the timing circuit; and
outputting a wordline decoder activation signal from the timing circuit based on the RAS* signal and the ISO signal.

10. The method according to claim 9, wherein outputting a wordline decoder activation signal includes activating an address select circuit in a wordline decoder.

11. The method according to claim 9, wherein outputting the wordline decoder activation signal includes only activating a wordline decoder after the ISO signal transitions to a low state.

12. The method according to claim 11, wherein outputting the wordline decoder activation signal includes only outputting an activation signal after RAS* transitions to a low state.

13. The method according to claim 12, wherein outputting the wordline decoder activation signal includes transitioning the RAS* signal low before the ISO signal transitions low such that outputting the activation signals is delayed until the ISO signal transitions low.

14. The method according to claim 9, wherein applying ISO signal to the timing circuit includes applying the ISO signal from a neighboring memory sub-array.

15. A method of activating a wordline in a memory device, comprising:

applying RAS* signal to a timing circuit;

delaying an ISO signal in a delay circuit;

applying the delayed ISO signal to the timing circuit; and

outputting from the timing circuit a wordline decoder activation signal based on the RAS* signal and the ISO signal.

16. The method according to claim 15, wherein delaying the ISO signal includes programming the delay time for the ISO signal.

17. The method according to claim 16, wherein outputting the wordline decoder activation signal includes only outputting the wordline decoder activation signal after the ISO signal transitions to a low state.

18. The method according to claim 17, wherein outputting the wordline decoder activation signal includes only outputting the wordline activation signal after RAS* transitions to a low state.

19. The method according to claim 18, wherein outputting the wordline decoder activation signal includes transitioning the RAS* signal low before the ISO signal transitions low such that outputting the activation signals is delayed until the ISO signal transitions low.

20. A method of controlling memory access in a memory device, comprising:

turning on first and second isolation circuits via first and second isolation signals to respectively conductively couple first and second pairs of digit lines to a sense amplifier;

transitioning the first isolation signal to a state opposite the state of the second isolation signal to isolate the first pair of digit lines from the sense amplifier;

locally connecting a timing circuit to a line carrying the first isolation signal; and

producing a wordline activation signal from the timing circuit after receipt of the change of state of the first isolation signal.

21. The method according to claim 20, wherein locally connecting the timing circuit includes maintaining a constant time differential from the time the first isolation circuit isolates the first pair of digit lines from the sense amplifier to when the wordline associated with the second isolation circuit is activated.

22. The method according to claim 20, wherein producing the wordline activation signal includes activating a wordline decoder until a row access signal transitions inactive.

23. The method according to claim 22, further comprising, during inactivation of the wordline decoder, transitioning the row access signal inactive before the first isolation signal transitions inactive at the local connection of the timing circuit to the line carrying the first isolation signal.

24. The method according to claim 22, wherein activating the wordline decoder until the row access signal transitions inactive includes inputting the row access signal into the timing circuit.

25. A method of controlling a wordline decoder in a memory device, comprising:

activating the wordline decoder based on the state of an isolation signal local to a memory array to be accessed; and

deactivating the wordline decoder based on the state of a row access signal.

26. The method according to claim 25, wherein activating the wordline decoder includes connecting the wordline decoder to a line carrying the isolation signal at a connection point close to an isolation gate adjacent the memory array to be accessed.

27. The method according to claim 25, wherein activating the wordline decoder includes inputting the isolation signal to a timing circuit and applying an output from the timing circuit to the wordline decoder.

28. The method according to claim 27, wherein activating the wordline decoder includes inputting the row access signal to the timing circuit and producing the output from the timing circuit based on the state of the isolation signal and the row access signal.

29. The method according to claim 28, wherein activating the wordline decoder includes inputting the row access signal before the isolation signal is received in the timing circuit.

30. The method according to claim 29, wherein deactivating the wordline decoder includes inputting an inactive row access signal before the isolation signal change is received in the timing circuit.

31. A method of controlling a wordline decoder in a memory device, comprising:

propagating a low active state isolation signal through a line in an integrated circuit to an isolation gate in a sense amplifier bank;

isolating a first memory array from the sense amplifier bank;

connecting a timing circuit to the line at a location local to a second memory array connected to the sense amplifier bank;

activating the wordline decoder by inputting an isolation signal into the timing circuit; and

deactivating the wordline decoder based on the state of a row access signal.

32. The method according to claim 31, wherein activating the wordline decoder includes first inputting the row access signal into the timing circuit and then inputting the isolation signal into the timing circuit.

33. The method according to claim 32, wherein activating the wordline decoder includes providing a row access signal and performing a NOR function in the timing circuit with the row access signal and the isolation signal as inputs.

34. The method according to claim 33, wherein activating the wordline decoder includes inputting both an output and an inverse output from the timing circuit to the wordline decoder.

35. The method according to claim 34, wherein activating the wordline decoder includes inputting the inverse output to an address decoding circuit in the wordline decoder and inputting the output to a latch circuit in the wordline decoder.

36. The method according to claim 33, wherein deactivating the wordline decoder includes shifting at least one of the isolation signal and the row access signal to a non-active state.

37. The method according to claim 33, wherein deactivating the wordline decoder includes shifting the row access signal to a high state.

38. A method of controlling a wordline decoder in a memory device, comprising:

propagating a low active state isolation signal through a line in an integrated circuit to an isolation gate in a sense amplifier bank;

isolating a first memory array from the sense amplifier bank;

connecting a timing circuit to the line at a location local to a second memory array connected to the sense amplifier bank; and

activating the wordline decoder by inputting a low active state isolation signal into the timing circuit.

39. The method according to claim 38, wherein activating the wordline decoder includes first inputting the row access signal into the timing circuit and then inputting the isolation signal into the timing circuit.

40. The method according to claim 39, wherein activating the wordline decoder includes providing a row access signal and performing a NOR function in the timing circuit with the row access signal and the isolation signal as inputs.

41. The method according to claim 40, wherein activating the wordline decoder includes inputting both an output and an inverse output from the timing circuit to the wordline decoder.

42. The method according to claim 41, wherein activating the wordline decoder includes inputting the inverse output to an address decoding circuit in the wordline decoder and inputting the output to a latch circuit in the wordline decoder.

43. A timing circuit, comprising:

an input adapted to receive at least one input signal, the at least one input signal including an isolation signal; and

an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal.

44. The timing circuit according to claim 43, wherein the at least one input signal includes a RAS* signal.

45. The timing circuit according to claim 44, wherein the output activates the address decoder based on a low RAS* signal and a low isolation signal.

46. The timing circuit according to claim 45, wherein the isolation signal is associated to a first memory array separate from a second memory array connected to the address decoder.

47. The timing circuit according to claim 43, wherein the input is connected to a NOR gate.

48. The timing circuit according to claim 43, wherein the input is connected to an AND gate.

49. A timing circuit connected to a wordline decoder of a first memory array, the timing circuit comprising:

an input adapted to receive at least one input signal, the at least one input signal including an isolation signal connected to a second memory array; and

an output connected to the wordline decoder, wherein the timing circuit activates the wordline decoder based on the at least one input signal.

50. The timing circuit according to claim 49, wherein the at least one input signal includes a RAS* signal.

51. The timing circuit according to claim 50, wherein the output activates the wordline decoder based on a low RAS* signal and a low isolation signal.

52. The timing circuit according to claim 49, wherein the input is connected to a NOR gate.

53. The timing circuit according to claim 49, wherein the input is connected to an AND gate.

54. The timing circuit according to claim 49, wherein the first memory and the second memory array are connected to one sense amplifier.

55. A memory device comprising:

a plurality of memory cells coupled to digit lines;

a sense amplifier;

a plurality of isolation gates coupled between the sense amplifier and the digit lines, the isolation gates being controlled by isolation signals;

a timing circuit connected to one of the plurality of isolation gates; and

a wordline decoder connected to the timing circuit and at least one of the memory cells, wherein the timing circuit triggers the wordline decoder upon a state change in isolation signal at the one isolation gate.

56. The memory device according to claim 55, wherein the timing circuit is connected to a RAS* signal and activates the wordline decoder based on both the isolation signal and the RAS* signal shifting low.

57. The memory according to claim 56, wherein the isolation signal experiences a delay from its source to the isolation gate relative to the RAS* signal.

58. A memory device comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

59. The memory device according to claim 58, wherein the first timing circuit receives a RAS* signal, and based on the RAS* signal and the state of the first isolation signal selectively activates the second wordline decoder.

60. The memory device according to claim 58, wherein the second isolation line transmits a second isolation signal to the second isolation gate, and a second timing circuit is connected to the second isolation line and the first wordline decoder and activates the first wordline decoder based on a change of state of the second isolation signal.

61. The memory device according to claim 60, wherein the second timing circuit receives a RAS* signal and based on the RAS* signal and the state of the second isolation signal selectively activates the first wordline decoder.

62. The memory device according to claim 60, wherein the plurality of sense amplifier banks includes N sense amplifier banks and N first isolation gates, plurality of memory arrays includes N * 2 memory arrays, and a number of first timing circuits equals N, and the number of second timing circuits is N.

63. The memory device according to claim 58, wherein the memory device is one of a DRAM, SRAM, Flash memory, SGRAM, SDRAM, SDRAM II, DDR SDRAM, Synchlink DRAM, and Rambus DRAM.

64. A computer, comprising:

a processor;

a plurality of memory arrays coupled to the processor, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

65. An integrated circuit, comprising:

a semiconductor wafer having first and second surfaces; and

a functional circuit formed on the first surface of the semiconductor wafer, the functional circuit including:

a plurality of memory arrays, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

66. An electronic system, comprising:

a processor; and

a memory coupled to the processor, the memory including:

a plurality of memory arrays, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

67. The electronic system according to claim 66, wherein the processor includes a user interface device.

68. A method of reducing data corruption in a memory device, comprising:

providing a timing circuit in the memory device;

connecting a wordline decoder to a memory array;

linking activation of the wordline decoder to the timing circuit; and

producing a wordline activation signal from the timing circuit based on a nearby ISO signal.

69. The method of claim 68, wherein producing the wordline activation signal includes relying on the physical arrival of the ISO signal and not on an estimate of the arrival of the ISO signal.